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A COMPARATIVE STUDY OF VEDIC 4-BIT MULTIPLIER USINGCMOS AND MGDI TECHNOLOGY

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ABSTRACT
In this article, a Vedic 4-bit multiplier is intended using CMOS and MGDI technologies. In essence, a well performing multiplier improves the efficiency of the system. In the current digital era, a multiplier is one that uses energy while also having a very significant impact on the situation. Multiplier optimization will be important for both power and delay. Additionally, adders are crucial to the multiplier. Here, the ripple carry adder is being used. In this project, gpdk 90nm technology is used in conjunction with the Cadence Virtuoso tool/Tanner EDA tool to implement the design. We execute transient results in this, considering the parameters of Area, Delay, and Maximum power.

Keywords: Vedic Multiplier, MGDI, CMOS, Ripple Carry Adder.

I. INTRODUCTION
The field of digital design and integrated circuits has seen a continuous evolution in technology and methodologies. Among these, CMOS and MGDI technologies have seen pivotal in shaping the landscape of digital circuit design. In the ever –evolving landscape of digital circuit design, the pursuit of faster, more efficient, and power-conscious arithmetic operations is a constant endeavour. One intriguing boulevard of the exploration in this field is the comparative study of 4-bit Vedic multipliers, a unique multiplication technique derived from ancient Indian mathematics. CMOS technology, widely adopted in the semiconductor industry, is known for its low power consumption and robust performance.

In contrast, MGDI technology, with its delay- insensitive nature, presents an intriguing alternative, especially in scenarios where energy efficiency is critical. The Frank Wanlass of Fairchild semiconductor came up with the concept for the CMOS process initially, and he and Chih-Tang Sah accessible it at the International Solid- State Circuits Conference in the year 1963. Subsequently, Wanlass filed for and was granted

U.S. Patent 3,356,858 for CMOS circuits in 1967. By using the Trademark “CMOS-MOS” to solidify this technology in the late 1960’s, RCA forced other manufacturers to come up with a different moniker, and by the early 1970’s “CMOS” had become the accepted term for the technology. In the 1980’s CMOS logic replaced transistor-transistor (TTL) technology of the predominant MOSFET production method for actual large-scale integration (VLSI) circuits, supplanting NMOS logic. The industry standard for fabricating MOSFET semiconductor devices in VLSI chips is still CMOS. In 2011 saw 99% of integrated circuits, comprising the majority of digital, analog, and mixed signal. Modified Gate Diffusion Input (MGDI) is an innovative digital circuit design technique that builds on traditional Gate Diffusion Input (GDI) technology. MGDI is attracting attention in the field of digital design for its ability to provide more compact and energy- efficient solutions for implementing complex logic function. As the demand for smaller, faster, and more energy- efficient digital circuits has grown, various design technologies.

II. LITERATURE REVIEW
To advance modern digital technology standards, it is necessary to support faster, better, and more optimized digital computing architectures. Based on Vedic calculation, the Vedic multiplier is unique of the quickest computation algorithms available today, facilitating high speed calculations. The current Vedic multiplier FPGA implementation is unable to optimize power consumption, latency, or area occupied. To attain the intended performance in rapports of LUTs, latency, and level power consumption, this article suggests modifying the Vedic multiplier design by employing add2 modules with various adder configurations. To effectively execute demand reduction performance measurement field, this is accomplished by slightly reorganizing the steering by altering the adder architecture modules utilized in the Vedic multiplier from 4-bits to 32-bits. In comparison conventional designs Vedic multipliers, the suggested design significantly reduced power consumption by 0.75-4.39%, latency by 3.27%, and LUT by 0.75-4.39. The proposed design was created using EDA Xilinx ISE tool in the Vivado design suite version 2017.2 and was coded in Verilog. The simulation results using the suggested design will be examined, presented, and concluded in this paper.

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III. EXISTING METHOD

In this paper, we designed the 4-bit Vedic multiplier using CMOS technology. Here, a Full Adder is designed using a Half Adder, an OR gate, 4-bit Vedic multiplier and Ripple Carry Adder. The circuitry of Vedic 2-bit multiplier consists of a half adder and an AND gate. Here, all the logic gates developed in this multiplier are of CMOS Logic gates only. One of the disadvantages in existing method is consuming more amount of power. The main drawback of existing methods is the increased power consumption due to the use of CMOS Logic.

IV. PROPOSED METHOD

In this paper, we used CMOS technology to design the Vedic 4- bit multiplier. Here, Vedic 4-bit multiplier is intended to Vedic 2-bit multiplier and Ripple Carry Adder circuit. The Ripple Carry Adder circuit is equipped a Full Adder circuit while Full Adder is equipped with two XOR gates and a MUX. The bit Vedic multiplier is equipped with an AND gate and a Half Adder circuit. Here, all logic gates developed in this multiplier are exclusively modified GDI Logic.

Fig.1 Block Illustration of Proposed Technique

The block illustration of proposed performance clearly shows the steps involved in this system which includes four steps. Fig.1 includes four steps to undergo the final output.

CMOS

For common sense functions, a formation of MOSFET fabrication technique known as complementary metal-oxide-semiconductor commonly identified as CMOS, employs complementary plus symmetrical pairing of p-type and n-type MOSFET. The CMOS is construct integrated circuit chips such as microprocessors, microcontrollers, memory chips (comprising CMOS BIOS), and additional common-sense circuits. The CMOS is utilized in equivalent circuits, including data converters, RF circuits (RF CMOS), photo sensors (CMOS sensors), and extraordinarily unified transceivers for numerous message applications. Two crucial features of CMOS are substantial noise resistance and minimal energy usage. The CMOS inverter, a simple circuit that combines a PMOS and NMOS transistor, is the fundamental virtual circuit block in CMOS VLSI layout.

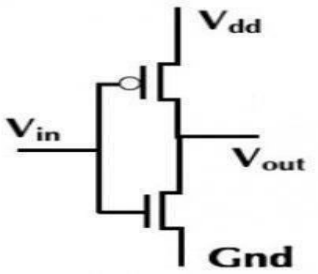

Fig.2 CMOS structure

In essence, this basic circuit is a NOT gate. Other basic logic gates can be created by combining MOSFET transistors, and these additional logic gates can then be combined to create larger logic circuits.

MGDI

MGDI constitutes an innovative method for constructing low-energy digital circuitry. The GDI technology is used in this procedure. MGDI constitutes a method for lessening power loss, the quantity of transistors, and the space of a digital circuit. Furthermore, MGDI includes three input terminals: G for PMOS input drain/source, P for PMOS input drain/source. However, PMOS bulk (SP) and NMOS (SN) are perpetually linked to VDD and GND, correspondingly.

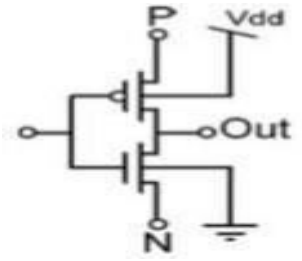

Fig.3 MGDI Structure

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2X2 BINARY MULTIPLIER

In electronic digital, similar an electrical circuitry within a computing machine, a binary multiplier could be employed to discover the outcomes of a pair of binary numerals. The binary multiplier is a copy of the conventional multiplication procedure; initiating with the slightest significant bit, each multiplier bit is multiplied. Pair semi-sum modules might be used to implement a 2- bit binary multiplier. Some of the recent computer arithmetic operations can be used to apply the number multiplier. Many of these techniques involve calculating a customary of limited goods and then summing the resulting limited goods.

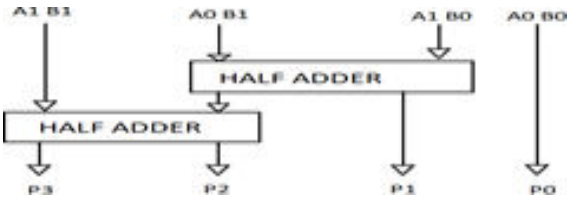

Fig.4 2x2 Binary Multiplier

4- BIT VEDIC MULTIPLIER

The 4x4 multiplication is performed on a single line in the Urdhva Tiryagbhyam sutra, while in the regular and conventional method, four partial product must added toget result. Therefore, by using the Urdhva Tiryagbhyam Sutra in binary multiplication, the numeral of steps required to compute the last invention will be abridged and thus will reduce the calculation time and increase inspeed of the multiplier.

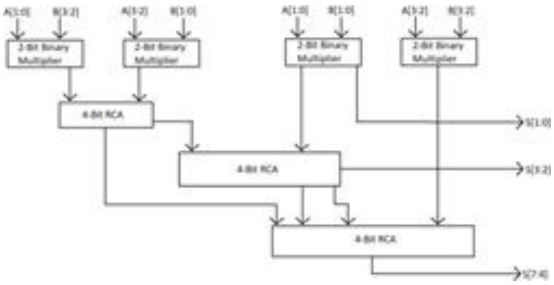

Fig.5 Vedic 4-bit Multiplier

The architecture of Vedic 4-bit multiplier using Vedic2- bit multiplier is integrated in Fig.5. The Multiplication process will be faster. Array multiplication is faster and uses less power than basic array multiplication. The whole speed and performance of the system are determined by the rate of summing and multiplication in the system. Because of the lengthy replication procedure, the delay will be greater. The multiplication is performed in three manners: Partial Product Generation (PPG), Partial Product Addition (PPA) and Final Convective Addition. The chief predicament is that should you wish to enhance the velocity of the multiplier partial outcomes, you need to diminish the outcome into segments. Vedic Mathematics concept we can ignore the carrier propagation delay. This system is based on 16 Vedas for which we use the Urdhva Tiryakbhyam Sutra (vertical and horizontal). Because the Vedic multiplier does not yield any partial products, the circuit can be made simpler by using fewer adders in the multiplier. The term Vedic is derivative as of name ―Veda which incomes of powerhouse of acquaintance. There are 16 sutras within Vedic math Urdhva Tiryakbhyam and Nikhilam Navatascaramam Dasatah are customarily used to build a multiplier and 13 sutras (sub formulas). Among the16 scriptures, the Urdhva Tiryakbhyam scripture was used to design the Vedic multiplier.

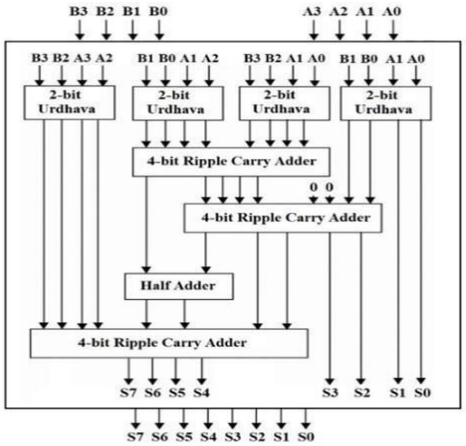

Fig.6 Architecture of Vedic 4-bit multiplier using Vedic 2-bit multipliers

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Inverting logic is very important in low-power circuit design. It allows you to determine output of input as well as input recovered from output. This is an n inputs and n outputs device with a one -to- one mapping. Invertible Logic has numerous applications, including Optical Computing, Quantum dot automata, and Low power architecture. In the operation of a normal logic circuit, when a little evidence is mislaid, it will consume energy. Lost Evidence cannot be recovered.

v. OUTPUT RESULT

For its Hiper Verify product line, Tanner EDA, a top supplier of integrated circuit design, authentication, and simulation software, is inspecting for an exceptional Senior Scientists/Developer. You will work with a group of professionals to develop cutting- edge algorithms for chip verification integrated circuits (DRC), layout abstraction, and layout contrasted with schematic (LVS) products.

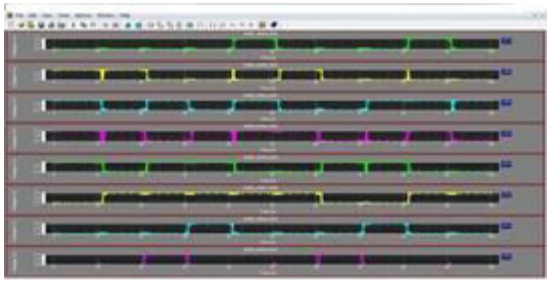

Fig.7 Simulation outcomes of Vedic 4x4 multiplier using CMOS.

The simulation outcomes of Vedic 4x4 multiplier using CMOS waveforms are represented for clear reference. Fig.8 Power outcome of Vedic 4x4 multiplier using CMOS provides the power optimization.

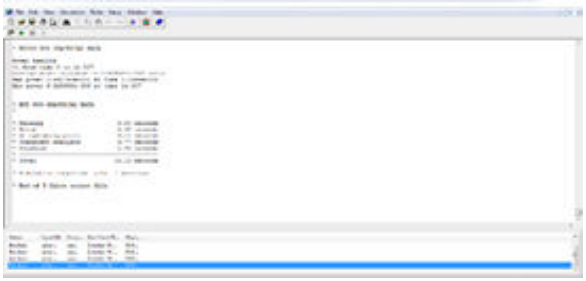

Fig.8 Power results of Vedic 4x4 multiplier usingCMOS.

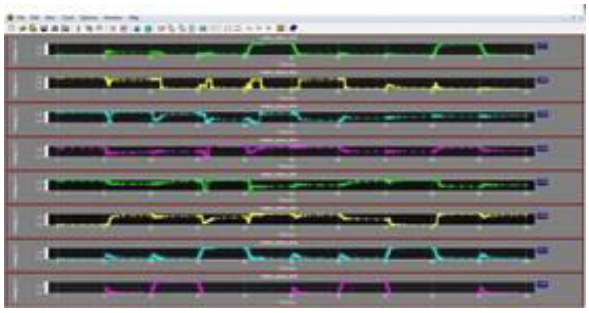

Fig.9 Simulation result of Vedic 4-bit multiplier usingMGDI.

The simulation result of Vedic 4-bit multiplier using MGDI waveform is represented for clear reference.Fig.10 Power result of Vedic 4x4 multiplier using MGDI provides the power estimation we can conclude comparatively lesser than existing method.

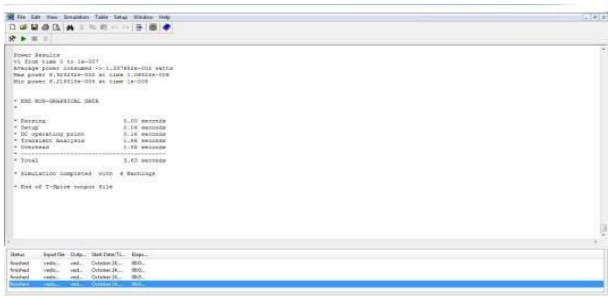

Fig.10 Power result of Vedic 4x4 multiplier using MGDI.

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VI. CONCLUSION AND FUTURE WORK

We mainly focus on developing Vedic multiplier with low power consumption and high presentation. MGDI and GDI cells offer digital designs that are superior to CMOS methodologies concerning efficiency and transistor amount. In a hindrance in Gate Diffusion Input method is that strong 0s and strong 1s cannot be obtained at the output for a specific combination of inputs. The MGDI technology mitigates this disadvantage. With just two transistors, you can implement an extensive variety of complex logic functions consuming the MGDI technique. Comparison of static CMOS and Domino CMOS based methods, MGDI gates minimize the quantity of transistors and the amount of silicon area needed. Compared to traditional logic styles, the MGDI gates have lower leakage power and hex power. Solving the GDI gate manufacturing problem in a standard nanoscale CMOS process involves using Mod-GDI logic style to connect the p- MOS and n-MOS sources to VDD and GND respectively. Our study of past research suggests that utilizing one of these low power digital designs has significant benefits. In conclusion, the proposed MGDI logic style-based design may be superior choice in future. The proposed multiplier is utilized in a varied series of applications and processors including DSP.

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